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ART UNIT	PAPER NUMBER
2614	13

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/191,629	TRAN ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-38,40-46,48-52 and 57-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *48-52* is/are allowed.

6)☒ Claim(s) *1-6,8-11,13-20, 22-38,40-46 and 57-61* is/are rejected.

7)☐ Claim(s) *12 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The indicated allowability of claims 8-33 is withdrawn in view of the newly discovered reference(s) to Dye, U.S. Pat. No. 6,067,098. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **8,10, 11,13-17, 25, 27-33** are rejected under 35 U.S.C. 102(e) as being anticipated by Dye, U.S. Pat. No. 6,067,098.

Considering claim 8, Dye discloses all claimed subject matter, note;

a) the claimed local bus is met by PCI/USB Fig.2A;

b) the claimed Digital television/local bus interface logic coupled to the local bus is met by Interactive Media Controller 140, fig.2A.

c) the claimed Digital television/local bus interface logic coupled to the local bus is met by Host I/F 202, fig. 6;

d) a local bus interface for transmitting outgoing digital television data over the local bus is met by HD_bus 207 and D_bus 2, fig.6;

e) a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner is met by Command FIFO/Data FIFO 205, fig.6;

f) second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner is met by Display storage FIFO 244, figs. 6 and 20;

g) the claimed memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer; digital television interface for receiving incoming digital television data, is met by Memory controllers 221 and 222, fig. 6;

Considering claim **10**, the claimed display device coupled to the local bus for receiving outgoing digital television data over the local bus is met by display 142, figs. 2A-2B.

Considering claim **11,** the claimed wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device is met by memory controllers 221 and 222, fig.6;

Considering claim **13**, the claimed wherein the local bus interface monitors a refresh of display device for receiving the outgoing digital television data is met by CPU 102, fig.2;

Considering claim **14**, the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

Regarding 14, see rejection of claim 1(d).

Considering claim **15**, the digital television local bus logic further comprising: a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer, is met by the disclosure that "Thus, the Graphics Engine 212 performs both graphical operations and screen refresh operations.... Instead, the Graphics Engine blocks are halted and the state of the machine is stored in the Temporary Registers 665. The refresh data, which could be any number of bits per pixel, is then shifted and property aligned for data into the display FIFO 244. Once the display FIFO 244 is full and ready for the refresh operation to occur out to the DACS, then the temporary storage registers 665 restore the prior context back into the engine, and the instruction which was suspended in the drawing procedure continues. Data traverses out of the color comparator block 660 and into the data out FIFO 263. The data out FIFO 263 is used to store information which is going to be written into a display memory areas in the system memory 110." (col. 46, line 57 through col. 47, line16)

Considering claim **16**, the claimed the digital television/local bus logic further comprising: a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

Regarding claim 16, see rejection of claim 15.

Considering claim **17**, a digital television/local bus interface logic, comprising:
a) the claimed a digital television interface for receiving incoming digital television data is met by the Host I/F 202, Fig.6;
b) the claimed a local bus interface for transmitting outgoing digital television data is met by PCI or USB, Fig. 2A;

c) the claimed a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner is met by the Command FIFO/data FIFO 205, Fig.6;

d) the claimed a second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner is met by Display Storage FIFO 244, fig.6;

e) the claimed a memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer on a first portion of a refresh of a display device and transmitting the outgoing digital television data in the one frame buffer to the display device on a second portion of the refresh of the display device is met by the Memory controllers 221 and 222, fig. 6;

Considering claim **25,** Dye discloses the following claimed subject matter, note;
a) the claimed a first interface means for receiving incoming digital television data is met by Host I/F 202, fig. 6;

b)a second interface means for transmitting outgoing digital television data by the 194/CCIR656 video in/out, fig. 3;

c) the claimed first buffer means for storing the incoming digital television data and the outgoing digital television data in an alternating manner is met by the Command FIFO/data FIFO 205, Fig.6;

d) a second buffer means for storing the outgoing digital television data and the incoming digital television data in an alternating manner is met by Display Storage FIFO 244, fig.6;

e) the claimed controller means for storing the incoming digital television data to one buffer means and reading the outgoing digital television data from another buffer means is met by CPU 102, fig.3;

Considering claim 27, the claimed the second interface means for transmitting the outgoing digital television data transmits the outgoing digital television data over a local bus is met by HD_bus 207, fig.6;

Considering claim 28, see rejection of claim 15.
Considering claim 29, see rejection of claim 16.

Considering claim 30, the claimed wherein the first interface means for receiving the incoming digital television data comprises a digital television interface.

Regarding claim 30, see rejection of claim 25 (a) and (b).

Considering claim 31, see rejection of claim 11.

Considering claim 32, see rejection of claim 12.

Considering claim 33, see rejection of claim 14.

4. Claims **57-61** are rejected under 35 U.S.C. 102(e) as being anticipated by **Johnson**, U.S. Pat. No. 6,330,038.

Considering claim **57**, Johnson discloses all claimed subject matter, note;
a) the claimed digital television/local bus interface logic for passing decoded digital television data is met video port 150, FIG.4;

b) the claimed a graphics controller for receiving the decoded digital television data over a local bus from the digital television/local bus interface logic is met graphics controller 154, FIG.4;

c) the claimed a display device for receiving the decoded digital television data from the graphics controller is met by Monitor 32 via VGA to Monitor interface 158.

Considering claim **58,** the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus is met by bus 108, Fig.3;

Considering claim **59**, the claimed a core logic for receiving the decoded digital television data from the digital television/local bus interface logic and passing the decoded digital television data to the graphics controller is met by video port 150, Fig.4;

Considering claim **60**, the claimed digital television decoder for providing decoded digital television data to the digital television/local bus interface logic is met by video decoder 146, FIG.4;

Considering claim **61**, the claimed digital television tuner for providing encoded digital television data to the digital television decoder is met by the disclosure that the A/V sub system 52 comprises two TV tuners, FIG.2;

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **1, 3-6,9, 18-20, 22-24, 26, 34-38, and 40-46 are** rejected under 35 U.S.C. 103(a) as being unpatentable over Dye, U.S. Patent No. 6,067,098.

Considering claim 1, Dye discloses the following claimed subject matter, note;

a) the claimed method of storing incoming digital television data in the first frame buffer is met by the Command FIFO/data FIFO 205, Fig.6;

b) the claimed method of reading outgoing digital television data from the second frame buffer is met by Display Storage FIFO 244, fig.6;

c) the claimed method of monitoring refresh of a display device coupled to the system is met by the CPU 102, fig.2

d) the claimed method of transmitting the outgoing digital television data in the second frame buffer to the display device when a programmed position of the display device is refreshed is met by the Display Storage FIFO 244, fig.6 and the Display Refresh List (VDRL) Engine 240 which "executes the video display refresh list". (col. 21, lines 22-25).

Except for;

e) the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

Regarding e), Dye does not specifically disclose that the refresh rate of the incoming digital television data is **decoupled** from a refresh rate of the outgoing digital television data. However, Dye discloses that "A graphics controller (IMC) which performs pointer-based and/or display list-based video refresh operations that enable screen refresh data to be assembled on a per window or per object basis, thereby greatly increasing the performance of the graphical display...This information is used during the screen refresh to display the various windows or objects on the screen very quickly and efficiently. Thus, the video display can be updated with new video data without requiring any system bus data transfers, which are required in prior art computer system architectures. The graphics controller dynamically adjusts the display refresh list for movement of objects and changes in relative depth priority which appear on the display...Rather, in many instances, either the video data for a respective window or object is changed, or only the pointers in the display refresh list are manipulated, to affect a screen change." (see Abstract)

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Dye by providing separate the refresh rate for the incoming data and transmitted data so that the display is independent of the

incoming refresh rate or that the display is not influenced by the incoming data's refresh rate in order to provide a smoother and more reliable display system.

Considering claim **3,** the claimed method of detecting whether the outgoing digital television data is stored in the first frame buffer or the second frame buffer, is met by the CPU 102, fig.2;

Considering claim **4**, the claimed method of monitoring step comprising the step of monitoring a horizontal sync and a vertical sync of the display device, is met by the discloses "The IMC 140 couples to a display device 142, such as a computer video monitor or television screen, among others. The IMC 140 generates appropriate video signals for driving display device 142. The IMC 140 preferably generates red, green, blue (RGB) signals as well as vertical and horizontal synchronization signals for generating images on the display 142. The IMC 140 also generates NTSC video signals, PAL video signals, or video signals for other analog or digital television/video formats. The IMC 140 may generate any of various types of signals for controlling a display device or video monitor. As shown, the IMC 140 preferably uses a serial control bus, such as the I2C serial bus, for control of the display device 142." (col. 10, lines 46-58)

Considering claim **5,** the claimed wherein the outgoing digital television data transmitted to the display device comprises a frame is met by the disclosure that "13) Digital display devices such as computer systems and digital televisions generally include a memory area, often referred to as a frame buffer, which stores the image or video portion which is currently being displayed. For example, in a computer system, the

frame buffer is typically stored in a separate VRAM memory, or in the system memory." (col.

Considering claim **6**, Dye discloses all claimed subject matter, except for;
The claimed method of transmitting the outgoing digital television data over a peripheral component interconnect (PCI) bus;

Regarding claim 6, Dye does not specifically disclose the PCI bus, however, Examiner takes Official Notice here in that the PCI bus connecting peripheral components or devices is well known in the art and therefore, would have been obvious to the skilled in the art.

Considering claim **9**, see rejection of claim 6.

Considering claim **18**, the claimed wherein the local bus interface comprises a peripheral component interconnect (PCI) interface is met by PCI, fig.2A.

Considering claim **19**, the claimed wherein the local bus interface transmits the outgoing digital television data over a local bus.

Regarding claim 19, see rejection of claim 6.

Considering claim **20,** see rejection of claim 11.

Considering claim **22,** see rejection of claim 14.
Considering claim **23,** see rejection of claim 15.
Considering claim **24,** see rejection of claim 16.

Considering claim 26, the claimed wherein the second interface means for transmitting the outgoing digital television data comprises a peripheral component interconnect (PCI) interface.

Regarding claim 26, see rejection of claim 6.

Considering claim **34**, Dye discloses all claimed subject matter, note;
c) the claimed a monitoring means for monitoring refresh of a display device is met by CPU 102, fig. 3;

d) the claimed a transmitting means for transmitting the outgoing digital television data in a storing means to the display device when a programmed position of the display device is refreshed, is met by Storage FIFO 244, fig.6;

Except for;
a) the claimed first storing means for storing the incoming digital television data and the outgoing digital television data in an alternating manner;
b) a second storing means for storing the outgoing digital television data and the incoming digital television data in an alternating manner;
e) the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

Regarding a) and b), Dye uses separate FIFO storage devices for storing incoming data and storing data. However, using a storage device for both incoming and outgoing data is well known in the art and thus, would have been obvious to the skilled in the art at the time the invention is made to modify the system of Dye so that one of

the FIFOs, for example, would be able to alternate between storing received data and transmitting it, in order to save storage space and cost.

Regarding e), see rejection of claim 1(e).

Considering claim **35**, a means for reading the outgoing digital television data from a storing means is met by display storage FIFO 244, fig.6;

Considering claim **36**, the claimed means for monitoring a horizontal sync and a vertical sync of the display device is met by the disclosure "The IMC 140 preferably generates red, green, blue (RGB) signals as well as vertical and horizontal synchronization signals for generating images on the display 142." (col. 10, lines 49-52)

Considering claim **37**, the claimed detecting means for detecting whether the outgoing digital television data is stored in the first storing means or the second storing means is met by CPU 102, FIG.3; (see also rejection of claim 34(a) and (b).

Considering claim **38**, see rejection of claim 6.

Considering claim **40**, Dye discloses the following claimed subject matter, note;
a) the claimed local bus is met by HD_bus 207, Fig. 6;

b)the claimed graphics controller coupled to the local bus is met Graphics Engine 212, fig. 6;

c)the claimed display device for receiving outgoing digital television data from the graphics controller is met by display 142, Fig. 2a;

d) the claimed digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed is met by Host I/F 202, fig.6;

Except for;

e) the claimed wherein the refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data;

Regarding e), see rejection of claim 1(e).

Considering claim **41**, the claimed a core logic coupled between the local bus and the graphics controller is met by Bus I/F logic 202, figs. 5 and 6;

Considering claim **42**, the claimed digital television decoder for providing incoming television data to the digital television/local bus interface logic is inherent in televisions system such as Dye's;

Considering claim **43**, the claimed digital television tuner for providing incoming digital television data to the digital television decoder, is inherent in televisions system such as Dye's;

Considering claim **44**, wherein the graphics controller provides **a feedback signa**l to the digital television/local bus interface logic to indicate whether the programmed position of the display device is refreshed, is met by the disclosure "The Graphics Engine 212 is stopped to enable the Graphics Engine 212 to perform the transfer of video data from the memory 110 to the video monitor 142, i.e. to actually fetch the display pixels, in addition to its bit blit duties. Thus the present invention uses the Graphics Engine 212 to actually load the display refresh mechanism. This is a novel use of the Graphics Engine 212 for both graphics and display refresh operations." (col. 58, lines 14-25)

Considering claim **45**, the claimed wherein the feedback signal comprises a horizontal sync and a vertical sync of the display device is inherent, because any video processing system would have horizontal sync and vertical sync signal in order to properly function or operate. (see also rejection of claim 36)

Considering claim **46**, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus.

Regarding claim 46, see rejection of claim 6.

Response to Arguments

Applicant's Arguments

a) Johnson fails to disclose or suggest a "digital television/local bus interface bus logic for passing decoded digital television data." The Office Action characterizes a video port 150 in Figure 4 of Johnson as the "digital television/local bus interface bus logic for

passing decoded digital television data." Figure 4, however, does not suggest that the video port 151 interfaces to a local bus or that the outgoing line 156 from the video port 151 is part of the local bus, thus there is no suggestion that the video port 150 is "digital television/local bus interface bus logic."

b) Figure 4 also fails to suggest that the incoming video signal 152 provided to the video port 150 is a digital video television signal, thus Figure 4 fails to suggest that the video port 150 is "digital television/local bus interface bus logic" in this respect as well.

Examiner's Response

a) Johnson discloses a Graphics subsystem/video subsystem 116 which interfaces with bus 108 through buses 126 and 128 (fig.3) Video decoder 146 (fig.4) decodes the video before sending it to Monitor through the Graphics controller 154 uses bus 124. "The bi-directional bus 126 couples the graphics subsystem 118 to the PCI bus 108, the bi-directional bus 128 couples the video subsystem 120 to the PCI bus 108." (col. 6, lines 56-59) And finally, Johnson clearly and uncompromisingly discloses, "In accordance with a further aspect of ***the present invention, there is provided a digital television system...***" [emphasis added] (see column 2, lines 55+) The video port 150 is clearly where the output of the video decoder 146 passes through to graphics controller 154.

Therefore, the argument that Johnson does not disclose a digital television/local bus interface bus logic is not persuasive.

b) the video decoder 146 converts the analog chrominance and luminance signals into a digital format , processes the signals independently, and provides the signals in the YUV format to the graphics subsystem. (col. 7, lines 20-24) Thus, the video signal 152 provided to Video port 150 is a digital television signal. Argument is unpersuasive.

Allowable Subject Matter

7. Claims **48-52** are allowed.

8. Claims **12** and **21** are/is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a method for transferring digital television data in a system having a first frame buffer and a second frame buffer comprising:

wherein the memory controller stores the incoming digital television data to the *second frame buffer* and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device, as in claims 12 and 21;

A memory controller for storing the first incoming digital television data stream to the first frame buffer or the second frame buffer and reading the first outgoing digital television data stream from the second frame buffer or the first frame buffer on a first

portion of a refresh of a display device, storing the second incoming digital television data stream to the third frame buffer or the fourth frame buffer and reading the second outgoing digital television data stream from the fourth frame buffer or the third frame buffer on the first portion of the refresh of the display device, transmitting the first outgoing digital television data stream to the display device on a second portion of the refresh of the display device, and transmitting the second outgoing digital television data stream to the display device on the second portion of the refresh of the display device, as in claim 48.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Baker et al., U.S. Patent No. 6,640,332 discloses a multimedia graphics system wherein words of different types of digital information, including standard interframe video (SIF), graphics, television and audio are transferred preferably in packets between a controller, storage memory and shift registers (e.g. FIFO's) individually associated with the different information types.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 6:30am -3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

Paulos Natnael
May 13, 2003

JOHN MILLER
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